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EXAMINER	
MAI, ANH D	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/254,939	Applicant(s) MIURA ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 November 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,12,13,15,18-39 and 41-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9, 10, 12, 13, 15, 18-39 and 41-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 3, 2003 has been entered.

Status of the Claims

2. Amendment filed November 3, 2003 has been entered. Claims 1, 2, 4, 5, 9, 10, 15, 39, 41-47 and 49-54 have been amended. Claims 1-6, 9, 10, 12, 13, 15, 18-39 and 41-55 are pending.

Claim Objections

3. Claim 3 is objected to because of the following informalities:

Claim 3, line 4 incorrectly recites: "<u>isotropic</u> etching" the correct process should be -- **anisotropic** etching --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Both claims , in line 2, recite: "**said providing** the curvature". However, there are two curvatures in Claim 10, namely: first curvature and increased curvature.

It is not known which "curvature" theses claims are directed to.

As best understood by the examiner, the curvature that includes bird's beak is the increased curvature.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims **1**, **9**, **10**, 12, 13, **15**, 18-20, 30-39, **41**, 42, 46-49 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta et al. (U.S. Patent No. 5,646,063) of record.

With respect to claim **1**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate (14); (Fig. 4);

(c) thermally oxidizing a trench portion formed in the semiconductor substrate (14), exposed in the trench (44) so as to form a first curvature of the upper end portion of the trench (44); (Fig. 5);

(d) burying a buried insulating film (60) into the trench (44) so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18); (Fig. 5);

(e) after burying the buried insulating film (60), removing the insulating film (60) on the oxidation prevention film (18), by chemical mechanical polishing (CMP), thereby forming a chemically mechanically polished surface (66); (Fig. 6);

(f) after the removing, performing selective thermal oxidation of the semiconductor substrate (14) after having formed the CMP polished surface (66), so as to thermally oxidize only a portion of the semiconductor substrate (14) at the upper end portion of the trench (44), and not substantially at other portion of the semiconductor substrate lining the trench (44), so as to increase a curvature of the upper end portion of the trench (44) substantially without oxidizing the other portions of the semiconductor substrate lining the trench (44); (Fig. 9);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

With respect to the limitation “thermally oxidizing”, the term “thermally grown” of Mehta (col. 5, ll. 30-35) is recognized in the art as thermally oxidizing. The thermal oxidation that form liner oxide (56) of Mehta is well known in the art to generate a bird’s beak at the

interface of the oxidation prevention film (18) and the upper corner of trench (44), thus, first curvature.

The "chemical mechanical planarization" of Mehta '063 is also known as chemical-mechanical polishing.

With respect to claims 18-20, the buried insulating film (60) of Mehta is made of silicon oxide formed by CVD .

With respect to claim **9**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming trench regions (44) in the substrate from the circuit formation surface thereof;

(c) performing a first thermal oxidation to form an oxide film (56) on the trench regions (44) formed in step (b), and to form a first curvature at upper end portions of trench regions (44) formed in step (b), and

(d) forming an insulating film (60) inside the thermally oxidized trench regions (44) so as to completely fill them, thereby forming completely filled trench regions, and forming the insulating film (60) on the oxidation prevention film (18),

(e) removing the insulating film (60) formed on the oxidation prevention film (18) by chemical mechanical polishing (CMP), thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing a second thermal oxidation, of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), so as to selectively oxidize only an opening side of the completely filled trench regions (44) in the substrate (14), and not substantially at other portions of the semiconductor substrate lining trench regions (44), substantially without oxidizing the other portions of the semiconductor substrate lining trench regions (44); and

(g) after performing the second thermal oxidation, removing the oxidation prevention film (18), and forming a gate oxide film (135). (See Figs. 1-9).

With respect to "thermally oxidizing" and "chemical mechanical planarization" the similar reasoning as that of claim 1 is also applied here.

With respect to claim **10**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate (14);

(c) thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench (44) so as to form a first curvature at upper end portion of trench (44);

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18) by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after removing, performing selective thermal oxidation of the semiconductor substrate (14), after having formed the chemically mechanically polished surface, so as to oxidize only apportion of the semiconductor substrate, at the upper end portion of the trench and not substantially at other portions of the semiconductor substrate lining the trench (44), to increase the curvature of the upper end portion of trench (44), substantially without oxidizing the other portions of the semiconductor substrate lining the trench (44); and

(g) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14). (See Figs. 1-9).

With respect to "thermally oxidizing" and "chemical mechanical planarization" the similar reasoning as that of claim 1 is also applied here.

With respect to claim 12, as best understood by the examiner, the increased curvature of Mehta includes forming a well known bird's beak at the upper end portion of the trench. (see Fig. 1).

With respect to claim 13, the increased curvature of Mehta is formed such that an angle (θ) between the circuit formation surface of the semiconductor substrate (14) and a side surface of the semiconductor substrate forming the trench is within a range of $90^\circ < \theta > 180^\circ$.

With respect to claims 49 and 52, the oxidation prevention film (18) of Mehta is eliminated or removed after thermally oxidizing only a portion of the semiconductor substrate.

With respect to claim **15**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in trench (44), so as to provide the upper end portion of the trench (44) with a curvature;

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), having the buried insulating film (60) in trench (44), by CMP thereby forming a chemically mechanically polished surface (66);

(f) after removing, performing selective thermal oxidation of semiconductor substrate (14), after having formed the chemically mechanically polished surface (66) only at the upper portion end portion of trench (44), to increase the curvature of the upper end portion of trench (44) as compared with the curvature provided in step (c), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44); and

(g) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14). (See Figs. 1-9).

With respect to "thermally oxidizing" and "chemical mechanical planarization" the similar reasoning as that of claim 1 is also applied here.

With respect to claims 18-20 and 30-38, the buried insulating film of Mehta is silicon oxide, deposited by CVD.

With respect to claim 39, the step (f) of removing the oxidation prevention film (18) of Mehta is performed after the performing thermal oxidation.

With respect to claim **41**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) thermally oxidizing a trench portion formed in the semiconductor substrate (14), exposed in trench (44), forming a curvature of the upper end portion of trench (44);

(d) burying a buried insulating film (60) into trench (44) so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing selective thermal oxidation of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), only at the upper end portion so as to provide an increased curvature of the upper end portion of trench (44) as compared with the curvature formed in step (c), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after the eliminating, forming a gate oxide film (135). (See Figs. 1-9).

With respect to "thermally oxidizing" and "chemical mechanical planarization" the similar reasoning as that of claim 1 is also applied here.

With respect to claim 42, step (g) of eliminating the oxidation prevention film (18) is performed after step (f) of selectively thermally oxidizing the semiconductor substrate (14) at the upper end portion.

With respect to claim **46**, Mehta '063 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench regions (44) in the substrate from the circuit formation surface thereof;

(c) performing a first thermal oxidation to form an oxide film (56) on trench regions (44) formed in step (b), so as to provide a curvature at an opening side of trench regions (44); and

(d) forming an insulating film (60) inside the thermally oxidized trench regions (44) so as to completely fill them, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing a selective second thermal oxidation of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66) to selectively oxidize only the opening side of the completely filled trench regions (44) in substrate (14) so as to provide an increased curvature at the opening side as compared to the curvature provided in step (c), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44); and

(g) after performing the second oxidation, removing the oxidation prevention film (18) and forming a gate oxide film (135). (See Figs. 1-9).

With respect to “thermally oxidizing” and “chemical mechanical planarization” the similar reasoning as that of claim 1 is also applied here.

With respect to claim **47**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined positions of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portions thereof extending to the circuit formation surface of the semiconductor substrate (14);

(c) thermally oxidizing a trench portions formed in semiconductor substrate (14), exposed in the trenches (44), there by providing the upper end portion of the trench with a radius curvature;

(d) burying a buried insulating film (60) into the trench (44) so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, providing the upper end portion of the trench (44) with an increased radius of curvature, as compared with the radius of curvature provided in step (c), by performing selective thermal oxidation only of the upper end portion of trench (44) of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44); and

(g) removing the oxidation film prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14). (See Figs. 1-9).

With respect to "thermally oxidizing" and "chemical mechanical planarization" the similar reasoning as that of claim 1 is also applied here.

With respect to claim 48, step (g) of eliminating or removing the oxidation prevention film (18) is performed after step (f) of selectively thermally oxidizing the semiconductor substrate (14) at the upper end portion or providing the upper end portion of the trench (44) with an increased radius of curvature.

6. Claims **2**-6, 21-29, **43**-45 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '063 in view of Takahashi (EU. Patent No. 0459397) of record.

With respect to claims **2** and **43**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(c) forming trenches (44) having a predetermined depth in semiconductor substrate (14);

(d) thermally oxidizing trench portions formed in the semiconductor substrate (14), exposed in the trenches (44), so as to form a radius curvature at the corners, at upper end portion of trenches (44);

(e) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(f) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(g) after the removing, performing selective thermal oxidation of semiconductor substrate (14), so as to oxidize only a portion of semiconductor substrate (14) extending from the corners, and not substantially at other portions of the semiconductor substrate lining trenches (44), so as to increase the radius of curvature of trenches (44), substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(h) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(i) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Thus, Mehta is shown to teach all the features of the claim with the exception of forming the trenches (44) using two steps etching.

However, Takahashi '397 teaches forming a trench using two steps etch including:

(b) forming shallow trenches (26) having a radius curvature (27) at the corners in a desired position of the circuit formation surface of a semiconductor substrate (22); (Fig. 2B);

(c) forming trench (28) having a predetermined depth to the shallow trenches (26) having a radius of curvature (27) so formed. (See Figs. 2A-C).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Mehta using two steps etching as taught by Takahashi to reduced leakage current.

With respect to claims **4** and **45**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming trench having a predetermined depth at a desired positions of the circuit formation surface of semiconductor substrate (14), the trench having an upper end portion;

(c) thermally oxidizing trench portions formed in semiconductor substrate (14), exposed in the trench, so as to forms a first curvature of the upper end portions of trenches (44);

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film(60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing selective thermal oxidation of semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), so as to oxidize only a portion of semiconductor substrate at the upper end portion of trenches (44), and not substantially at other portions of the semiconductor substrate lining trenches (44), the upper end portions being oxidized, so as to increase a curvature of the upper end portions of trenches (44), substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(g) removing the oxidation preventing film (18) formed on the circuit formation surface of the semiconductor substrate (14); and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of trenches having upper end portions not covered by the oxidation prevention film, the similar reasoning as that of claims **2** and **43** is also applied here. Note that, forming trenches by two step etching of Takahashi is result in trench (28) having upper end portion (27) not covered by the oxidation prevention film (23). (See Fig. 2C).

With respect to claim **5**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(c) forming trenches (44) having a predetermined depth in semiconductor substrate (14);

(d) thermally oxidizing trench portions formed in the semiconductor substrate (14), exposed in the trenches (44), so as to form a radius of curvature of the corner, at upper end portions of trench (44);

(e) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(f) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(g) after the removing, performing selective thermal oxidation of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), so as to oxidize only a portion of the semiconductor substrate extending from the corners, and not substantially at other portions of the semiconductor substrate lining trenches (44), so as to

increase the radius of curvature of the trenches corner, substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(h) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14); and

(i) after the thermally oxidizing the semiconductor substrate (14), forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of shallow trenches having radius of curvature, the similar reasoning as that of claims **2** and **43** is also applied here.

With respect to claims 3, 6, the step for forming shallow trenches (26) of Takahashi is carried out by isotropic etching and the step of forming trenches (28) is carried out by anisotropic etching to a predetermined depth.

With respect to claims 21-29, the buried insulating film (60) of Mehta is silicon oxide, deposited by CVD.

With respect to claim 44, step (h) of Mehta is performed after step (g).

With respect to claim 51, the oxidation prevention film (18) of Mehta '063 is removed after the oxidizing only portion of the semiconductor substrate.

With respect to claims 50 and 53, the oxidation prevention film (120) of Mehta '599 is removed after the oxidizing only portion of the semiconductor substrate.

With respect to claim **54**, Mehta '063 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate (14), trench (44) being formed by anisotropic etching the semiconductor substrate (14);

(c) thermally oxidizing the trench portions formed in the semiconductor substrate (14), exposed in the trenches (44);

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) after burying the buried insulating film(60), performing an additional thermal oxidation so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench (44), to increase the radius of curvature in the proximity of the upper end portion of trench (44), and substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(f) after burying the buried insulating film (60), removing the insulating film (60) on the oxidation prevention film (18);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of trench using two steps etching, the similar reasoning as that of claims **2** and **43** is also applied here. Note that, trench (28) of Takahashi is formed by first etch using isotropic etching to form trench (26), so as to form a radius of curvature in the proximity of the upper end portion, and by the second etch using anisotropic etching to form trench (28). (See Figs. 2A-C).

With respect to claim 55, performing an additional thermal oxidation of Mehta is performed after removing the insulating film (60) on the oxidation prevention film (18).

Response to Arguments

7. Applicant's arguments filed November 3, 2003 have been fully considered but they are not persuasive.

Applicants argue that the applied references have neither taught not would have suggest such a method as in the amended claims including: after forming a trench or trench region, thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench, so as to form, e.g., a first curvature of the upper end portions of the trench, and after burying a buried insulating film into the trench and on an oxidation prevention film on a substrate having the trench formed therein, removing the insulating film by chemical mechanical polishing and thereafter performing selective or additional thermal oxidation of the substrate after having formed the chemically mechanically polished surface, so as to thermally oxidize only a portion of the substrate, at the upper end portion of the trench, and not substantially at other portions of the substrate lining the trench, so as to increase a curvature of the upper end

portion of the trench substantially without oxidizing the other portions of the semiconductor substrate lining the trench.

All of these element are clearly taught by Mehta. (See rejection above).

1) with respect to "thermally oxidizing a trench portion", the liner oxide 56 is formed by **thermally grown**, hence, thermally oxidizing. One having ordinary skill in the art would have known this. The formation of "curvature of the upper end portion" or rounding of the corner by forming thermal liner are well documented. Applicants are urged to sturdy C.P Chang et al. (PTO 892, paper # 14).

2) with respect to "after burying a buried insulating film into the trench and on an oxidation prevention film on a substrate having the trench formed therein, removing the insulating film by chemical mechanical polishing", see Mehta's Fig. 6. Applicants appear to not fully understand that <u>chemical mechanical planarization</u> is the same as <u>chemical mechanical polishing</u>.

3) with respect to "and thereafter performing selective or additional thermal oxidation of the substrate <u>after having formed the chemically mechanically polished surface</u>", Mehta teaches "After layer 60 is subjected to an oxide etch, structure 12 is subjected to thermal oxidation to grow the oxide in spacing 44" (see col. 5, ll. 54-56). Note that, the thermal oxidation is performed after the chemically mechanically polished surface 66 have been formed, thus, encompasses the claimed. Also note that, the additional thermal oxidation of Mehta only oxidize the upper end portion of trench (44) thus, forming the bird's beak, thus, increase the curvature (formed by thermal liner) of the upper end portion and the rest of trench (44) still remained. (See Fig. 9).

Applicants also added: and in fact would have taught away from, the method. It appears that that the Applicants fails to identify which portions that taught away from the invention as claimed.

With respect to two steps etching, Takahashi clearly teaches that.

The remaining arguments only a repetition of the previous argument, thus, the same response is applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575 or after January 13, 2004 please use (571) 272-1710. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
December 18, 2003